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From Silicon to Sovereignty: A Public Policy and Regulatory Framework for India's Semiconductor Decade

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ABSTRACT

Semiconductors have become an object of explicit industrial policy rather than ordinary trade, and India, having built three decades of growth on software services rather than hardware, now seeks to anchor itself in the semiconductor value chain through the India Semiconductor Mission and its financial outlay of the order of ten billion United States dollars. This paper argues that the binding constraint on India's semiconductor ambition is not the generosity of its incentives but the reliability of its execution, so that the decisive reforms are legal, institutional and administrative rather than fiscal. Drawing on doctrinal legal research, comparative policy analysis and the experience of Taiwan, South Korea, the United States and the European Union, it maps the obstacles that lie between aspiration and operational reality: regulatory proliferation and the limits of the single window, water and power constraints, an inadequate intellectual-property framework, an acute shortage of specialised talent, and weak Centre-State coordination. It then proposes an implementation-oriented public-policy and regulatory framework, organised by horizon, spanning time-bound deemed-approval clearances, a fast-tracked environmental-clearance category, operationalisation of the layout-design regime, a standalone trade-secrets statute, a national semiconductor talent programme, and a standing intergovernmental coordination council with performance-conditioned incentive disbursement. The analysis distinguishes verified empirical claims, each sourced in the notes, from the author's interpretive arguments, and concludes that whether India converts its finite window into durable capability depends on the coordinated urgency of its bureaucracies, courts, universities and State governments.

Keywords: *Semiconductors, India Semiconductor Mission, industrial policy, semiconductor regulation, intellectual property, trade secrets, technology transfer, Centre-State coordination, talent development, technology sovereignty.*

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I. INTRODUCTION

Few classes of manufactured goods carry the strategic weight of the semiconductor. Integrated circuits are embedded in consumer electronics, automobiles, medical devices, communications networks, energy infrastructure and defence platforms, and control over their supply chains now confers leverage over economic resilience and national security as much as over commercial markets. The fragility of those supply chains, exposed by the disruptions of the early 2020s, has driven the world's largest economies to treat semiconductors as an object of explicit industrial policy rather than ordinary trade.¹

India approaches this contest from an unusual position. Having built three decades of growth on software services rather than hardware, it now seeks to anchor itself in the semiconductor value chain through the India Semiconductor Mission (ISM), launched under the Ministry of Electronics and Information Technology with a financial outlay of ₹76,000 crore, of the order of ten billion United States dollars, to catalyse fabrication, assembly, testing and design capability on Indian soil.² This is among the most ambitious industrial-policy commitments the country has made in a generation.

Yet ambition is not architecture. Between the aspiration of a self-reliant semiconductor industry and the operational reality of running a fabrication plant lie a series of formidable obstacles: regulatory proliferation, water and power constraints, gaps in intellectual-property protection, an acute shortage of specialised talent, and persistent coordination difficulties between the Union and the States. This paper maps those obstacles and proposes an implementation-oriented public-policy and regulatory framework intended to convert India's semiconductor aspiration into durable capability. It addresses the full policy stack, from single-window clearances and environmental norms to intellectual-property reform, talent formation and Centre-State fiscal compacts, and it draws on the comparative experience of Taiwan, South Korea, the United States and the European Union, calibrated to India's federal structure and developmental context. The argument throughout is that the binding constraint on India's semiconductor ambition is not the generosity of its incentives but the reliability of its execution, and that the relevant reforms are therefore primarily legal, institutional and administrative. The analysis combines doctrinal legal research, comparative policy analysis and regulatory analysis, and

¹ Chad P. Bown & Dan Wang, *Semiconductors and Modern Industrial Policy*, 38 J. Econ. Persp. 81, 81-110 (2024).

² India Semiconductor Mission, *About SemiconIndia Programme*, Ministry of Electronics & Information Technology, Govt. of India, <https://ism.gov.in/about-semiconindia> (last visited June 2026); Ministry of External Affairs (Econ. Diplomacy Div.), *India's Semiconductor Market Set to Reach \$103.4 Billion by 2030*, IndBiz, Govt. of India (Feb. 12, 2025), <https://indbiz.gov.in/indias-semiconductor-market-set-to-reach-103-4-billion-by-2030/>.

distinguishes verified empirical claims, each sourced in the notes, from the author's interpretive arguments.

II. WHY SEMICONDUCTORS MATTER

Semiconductors are not simply another category of manufactured goods; they are the foundational substrate of the digital economy, of modern defence systems, of clean-energy infrastructure and of advanced healthcare. Their strategic significance for India operates across three dimensions, economic, security and technological, each of which independently justifies a serious industrial-policy response.

A. Economic multiplier effects

The scale of the global market is the first consideration. Worldwide semiconductor sales reached approximately USD 574 billion in 2022, the highest annual total recorded to that point, and credible industry analysis projects the sector to approach one trillion dollars by 2030.³ More important than the headline figure is the value-addition the industry anchors downstream: fabrication capacity catalyses far larger volumes of electronics manufacturing and digital-services activity. For India, the demand side is already substantial. Official figures place the domestic semiconductor market at roughly USD 52 billion in 2024-25, project it to reach USD 103.4 billion by 2030, and describe it as powering an electronics industry exceeding USD 400 billion; the same source records that companies committed more than USD 21 billion to semiconductor projects in the preceding year.⁴ Domestic production therefore represents both an import-substitution opportunity and a potential export engine.

B. National security and strategic autonomy

Modern defence platforms, from combat aircraft and missile systems to surveillance and battlefield-communication networks, depend on advanced semiconductors. A country that cannot produce or reliably source the chips its defence establishment requires is strategically exposed in a manner analogous to one that cannot secure its own food or fuel. The supply disruptions of the pandemic period demonstrated how a technological chokepoint can translate rapidly into operational vulnerability across both civilian and military systems. Strategic

³ Semiconductor Indus. Ass'n, *2023 State of the U.S. Semiconductor Industry* (2023), https://www.semiconductors.org/wp-content/uploads/2023/08/SIA_State-of-Industry-Report_2023_Final_080323.pdf; Ondrej Burkacky, Julia Dragon & Nikolaus Lehmann, *The Semiconductor Decade: A Trillion-Dollar Industry*, McKinsey & Co. (Apr. 1, 2022), <https://www.mckinsey.com/industries/semiconductors/our-insights/the-semiconductor-decade-a-trillion-dollar-industry>.

⁴ Ministry of External Affairs (Econ. Diplomacy Div.), *India's Semiconductor Market Set to Reach \$103.4 Billion by 2030*, IndBiz, Govt. of India (Feb. 12, 2025), <https://indbiz.gov.in/indias-semiconductor-market-set-to-reach-103-4-billion-by-2030/>.

autonomy in the semiconductor domain is thus not merely an economic aspiration but a national-security imperative, and it is the dimension on which the case for domestic capability is least susceptible to purely commercial cost-benefit analysis.

C. Technology sovereignty and the artificial-intelligence imperative

The artificial-intelligence transition has created intense demand for specialised compute, graphics processing units, tensor processing units and application-specific integrated circuits, so that control over chip supply chains increasingly shapes the pace and direction of AI development itself. India's ambition to be a significant participant in artificial intelligence cannot be realised without either a credible domestic semiconductor ecosystem or, at minimum, secure and diversified access to global supply. This linkage between compute and capability is the reason that semiconductor policy can no longer be treated as a sectoral concern; it is foundational to the broader technological sovereignty on which a range of national objectives now depends.

III. GLOBAL SEMICONDUCTOR GEOPOLITICS

The semiconductor industry is undergoing its most consequential restructuring since the 1980s, driven by the convergence of great-power competition, the supply-chain fragility revealed by the pandemic, and the demands of artificial intelligence and advanced computing. Positioning India's response requires an appreciation of this landscape.

A. The United States-China technology contest

The United States has enacted an unprecedented sequence of export controls restricting China's access to advanced computing chips and to semiconductor-manufacturing equipment. The Bureau of Industry and Security's rule of October 2022, expanded in October 2023, amended the Export Administration Regulations to control advanced computing integrated circuits and certain manufacturing items, together with the supercomputer and semiconductor end-uses associated with them.⁵ In parallel, the CHIPS and Science Act of 2022 committed substantial federal resources to onshoring manufacturing, approximately USD 39 billion in direct fabrication incentives within a broader package the Department of Commerce accounts at USD 52.7 billion, alongside a twenty-five per cent advanced-manufacturing investment tax credit.⁶

⁵ Implementation of Additional Export Controls: Certain Advanced Computing and Semiconductor Manufacturing Items; Supercomputer and Semiconductor End Use; Entity List Modification, 87 Fed. Reg. 62186 (Oct. 13, 2022), <https://www.federalregister.gov/documents/2022/10/13/2022-21658/implementation-of-additional-export-controls-certain-advanced-computing-and-semiconductor>.

⁶ CHIPS and Science Act of 2022, Pub. L. No. 117-167, 136 Stat. 1366 (2022), <https://www.govinfo.gov/content/pkg/PLAW-117publ167/html/PLAW-117publ167.htm>; Nat'l Inst. of Standards & Tech., *CHIPS for America Fact Sheet: Federal Programs Supporting the U.S. Semiconductor Supply Chain and*

These measures have begun to fragment a previously integrated global supply chain into competing technological blocs, compelling other nations to navigate carefully between ecosystems defined by allied export-control regimes on one side and Chinese indigenous alternatives on the other.⁷

The trajectory of China's own self-sufficiency drive offers a cautionary lesson for any subsidy-led strategy. Despite an estimated USD 150 billion in cumulative public funding under the Made in China 2025 framework, which set a seventy per cent localisation target, domestically produced chips accounted for only about thirty per cent of Chinese consumption in 2025, and the country's integrated-circuit output fell by 9.8 per cent in 2022 following the imposition of allied export controls.⁸ The episode demonstrates that the scale of funding is not, by itself, determinative: the binding constraints, access to leading-edge equipment and process know-how, and the maturity of the surrounding ecosystem, are not soluble by capital alone, a conclusion of direct relevance to India's calibration of its own programme.

B. Taiwan's pivotal role and its risks

The structural vulnerability of the system is concentrated in Taiwan. In 2021 the island accounted for roughly twenty-one per cent of global semiconductor manufacturing capacity but ninety-two per cent of capacity for the most advanced chips, and its foundries collectively supplied close to seventy per cent of global foundry revenue in early 2023; TSMC alone accounted for fifty-four per cent of global foundry revenue in 2020.⁹ Independent supply-chain analysis confirms that the entirety of sub-ten-nanometre capacity sits in Taiwan and South Korea.¹⁰ This concentration converts an ordinary commercial dependency into a systemic risk, because disruption at a single geographic node, whether through conflict, blockade or extended

Workforce, U.S. Dep't of Commerce (2024), <https://www.nist.gov/document/chips-america-fact-sheet-federal-incentives>.

⁷ Sujai Shivakumar, Charles Wessner & Thomas Howell, *China's Localization Drive in Semiconductors Gains Impetus from Allied Chip Export Controls*, Ctr. for Strategic & Int'l Studies (Mar. 24, 2026), <https://www.csis.org/analysis/chinas-localization-drive-semiconductors-gains-impetus-allied-chip-export-controls>.

⁸ Sujai Shivakumar, Charles Wessner & Thomas Howell, *China's Localization Drive in Semiconductors Gains Impetus from Allied Chip Export Controls*, Ctr. for Strategic & Int'l Studies (Mar. 24, 2026), <https://www.csis.org/analysis/chinas-localization-drive-semiconductors-gains-impetus-allied-chip-export-controls>.

⁹ Lin Jones & Samantha Krulikowski, *Taiwan—The Silicon Island*, U.S. Int'l Trade Comm'n, Off. of Econ., Exec. Briefing on Trade (Feb. 2024), https://www.usitc.gov/publications/332/executive_briefings/ebot_silicon_island_taiwan_semiconductor.pdf; Gregory Arcuri & Sujai Lu, *Taiwan's Semiconductor Dominance: Implications for Cross-Strait Relations and the Prospect of Forceful Unification*, Ctr. for Strategic & Int'l Studies (Mar. 22, 2022), <https://www.csis.org/blogs/perspectives-innovation/taiwans-semiconductor-dominance-implications-cross-strait-relations>.

¹⁰ Semiconductor Indus. Ass'n & Bos. Consulting Grp., *Strengthening the Global Semiconductor Supply Chain in an Uncertain Era* (2021), <https://www.semiconductors.org/strengthening-the-global-semiconductor-supply-chain-in-an-uncertain-era/>.

political tension in the Taiwan Strait, would cascade through automotive, defence, consumer-electronics and data-centre supply chains within weeks. The mitigation of this so-called Taiwan concentration has become a central preoccupation of industrial policy in the United States, Europe, Japan and Korea.¹¹

C. The friend-shoring opportunity and its time limits

The drive among the United States, the European Union, Japan, South Korea and their partners to diversify supply chains away from geopolitically sensitive concentrations creates a genuine opening for India. As a large democracy with an established engineering workforce and deep existing relationships with global technology firms through its software sector, India is well placed to attract a share of relocating investment, provided its policy environment is credibly competitive. That qualification is decisive, because the same capital is being courted by other jurisdictions, and the window is therefore real but time-limited; the determinant of success is the speed and reliability of policy execution rather than the announcement of intent.

D. Institutional frameworks: iCET and the Quad

India's diplomatic positioning has created preferential channels for technology cooperation. The United States-India initiative on Critical and Emerging Technology (iCET), whose inaugural meeting was held in January 2023, contains a dedicated semiconductor track, with the two governments committing to collaborate on resilient supply chains and on the development of a design, manufacturing and fabrication ecosystem in India, and welcoming an industry task force convened by the United States and Indian semiconductor associations.¹² Within the Quadrilateral grouping, leaders subsequently finalised a Memorandum of Cooperation establishing a Semiconductor Supply Chains Contingency Network to address supply-chain risks.¹³ These frameworks offer India access to technology and markets that would otherwise be difficult to obtain, but they are reciprocal arrangements: their benefits are contingent on India's credibility on intellectual-property protection and export-control discipline, which returns the analysis to questions of domestic legal and regulatory execution.

¹¹ William A. Reinsch & Jack Whitney, *Silicon Island: Assessing Taiwan's Importance to U.S. Economic Growth and Security*, Ctr. for Strategic & Int'l Studies (Jan. 10, 2025), <https://www.csis.org/analysis/silicon-island-assessing-taiwans-importance-us-economic-growth-and-security>.

¹² The White House, *Fact Sheet: United States and India Elevate Strategic Partnership with the Initiative on Critical and Emerging Technology (iCET)* (Jan. 31, 2023), <https://bidenwhitehouse.archives.gov/briefing-room/statements-releases/2023/01/31/fact-sheet-united-states-and-india-elevate-strategic-partnership-with-the-initiative-on-critical-and-emerging-technology-icet/>.

¹³ The White House, *Fact Sheet: 2024 Quad Leaders' Summit* (Sept. 21, 2024), <https://bidenwhitehouse.archives.gov/briefing-room/statements-releases/2024/09/21/fact-sheet-2024-quad-leaders-summit/>.

IV. INDIA'S SEMICONDUCTOR MISSION

The India Semiconductor Mission, notified in December 2021 and operationalised over the following years, marks a decisive departure from the country's historically passive approach to advanced manufacturing. It establishes an incentive architecture designed to attract semiconductor and display fabrication, compound-semiconductor and sensor fabrication, and assembly, testing, marking and packaging (ATMP/OSAT) facilities, alongside a programme for chip design.¹⁴

A. The incentive architecture

The programme offers fiscal support of up to fifty per cent of project cost for semiconductor fabs, display fabs and compound-semiconductor and sensor fabs, and up to fifty per cent of capital expenditure for ATMP/OSAT facilities, complemented by a Design Linked Incentive providing up to fifty per cent of eligible expenditure for design firms together with a deployment-linked incentive on net sales.¹⁵ The structure is generous by international standards and was deliberately calibrated to neutralise the first-mover disadvantage that a late entrant faces against established clusters. Its design is sound; the difficulty, as the remainder of this paper argues, lies less in the incentive than in the surrounding execution environment.

B. Early approvals and progress

The project pipeline demonstrates real traction. Micron's assembly and test facility at Sanand, Gujarat, approved in June 2023 with capital investment of ₹22,516 crore (about USD 2.75 billion) and fifty per cent fiscal support, commenced commercial production in February 2026.¹⁶ In February 2024 the Union Cabinet approved three further units: a Tata Electronics-Powerchip fabrication plant at Dholera, Gujarat (₹91,000 crore, 28-nanometre process, 50,000 wafer starts per month); a Tata assembly and test facility at Morigaon, Assam (₹27,000 crore); and a CG Power-Renesas-Stars Microelectronics assembly unit at Sanand (₹7,600 crore).¹⁷ Kaynes Semicon's Sanand unit (₹3,300 crore) followed in September 2024, and by May 2026

¹⁴ India Semiconductor Mission, *About SemiconIndia Programme*, Ministry of Electronics & Information Technology, Govt. of India, <https://ism.gov.in/about-semiconindia> (last visited June 2026).

¹⁵ Ministry of Electronics & Info. Tech., *Government of India Taking Steps to Encourage Domestic Manufacturing of Semiconductors*, Press Info. Bureau, Govt. of India (July 31, 2024), <https://www.pib.gov.in/PressReleaseIframePage.aspx?PRID=2039638>.

¹⁶ Ministry of Electronics & Info. Tech., *Micron's Semiconductor Project at Sanand in Gujarat on Fast Track*, Press Info. Bureau, Govt. of India (Dec. 6, 2023), <https://www.pib.gov.in/PressReleaseIframePage.aspx?PRID=1983128>; Prime Minister's Office, *Prime Minister Inaugurates Micron Technology's Semiconductor ATMP Facility in Sanand, Gujarat*, Press Info. Bureau, Govt. of India (Feb. 28, 2026), <https://www.pib.gov.in/PressReleasePage.aspx?PRID=2233998>.

¹⁷ Union Cabinet, *Giant Leap for India Semiconductor Mission: Cabinet Approves Three More Semiconductor Units*, Press Info. Bureau, Govt. of India (Feb. 29, 2024), <https://www.pib.gov.in/PressReleasePage.aspx?PRID=2010132>.

the cumulative tally had reached twelve approved projects representing roughly ₹1.64 lakh crore of investment.¹⁸ This is a significant start, though still modest against the scale of competing jurisdictions.

The mission has also begun to extend beyond fabrication into the upstream design ecosystem and to signal continuity through a successor phase, with design-infrastructure support extended to a large number of academic institutions and start-ups and the modernisation of the legacy Semi-Conductor Laboratory approved as a brownfield facility.¹⁹ This breadth is appropriate, since fabrication capacity in isolation would leave India dependent on imported design and supply; but it also multiplies the regulatory and coordination touchpoints the state must manage well, reinforcing rather than relieving the emphasis on execution that this paper develops.

C. Gaps in the current framework

Well-designed though its incentive structure is, the mission exhibits gaps that lie outside the fiscal instrument and that this paper addresses in turn. The single-window mechanism has convening influence but not decisional authority over line ministries; environmental-clearance processes are not calibrated to the specific profile of a water-intensive fab; the intellectual-property framework is not yet sufficient to reassure technology-intensive investors; the pipeline of semiconductor-specialised engineers is critically thin; and Centre-State coordination on land, power, water and industrial infrastructure lacks binding accountability mechanisms. Each of these is a problem of execution rather than of policy conception, and each is examined below.

V. REGULATORY BOTTLENECKS

India's regulatory environment, despite a decade of ease-of-doing-business reform, remains a formidable obstacle for capital-intensive manufacturing at semiconductor scale. A fabrication plant is unlike a conventional factory: it requires a large number of discrete permits, employs novel chemical processes, generates specific hazardous-waste streams, and must operate continuously without regulatory interruption.

¹⁸ Ministry of Electronics & Info. Tech., *Cabinet Approves One More Semiconductor Unit Under India Semiconductor Mission (ISM)*, Press Info. Bureau, Govt. of India (Sept. 2, 2024), <https://www.pib.gov.in/PressReleaseIframePage.aspx?PRID=2050859>; Ministry of Electronics & Info. Tech., *Cabinet Approves Two More Semiconductor Manufacturing Units*, Press Info. Bureau, Govt. of India (May 5, 2026), <https://www.pib.gov.in/PressReleasePage.aspx?PRID=2258119>.

¹⁹ Ministry of Electronics & Info. Tech., *Government of India Taking Steps to Encourage Domestic Manufacturing of Semiconductors*, Press Info. Bureau, Govt. of India (July 31, 2024), <https://www.pib.gov.in/PressReleaseIframePage.aspx?PRID=2039638>; Prime Minister's Office, *Prime Minister Inaugurates Micron Technology's Semiconductor ATMP Facility in Sanand, Gujarat*, Press Info. Bureau, Govt. of India (Feb. 28, 2026), <https://www.pib.gov.in/PressReleasePage.aspx?PRID=2233998>.

A. The proliferation of permits

A fab seeking to establish operations in India must navigate, at a minimum, environmental clearance under the regime administered by the Ministry of Environment, Forest and Climate Change; consents to establish and operate from central and state pollution-control boards; land allotment from state industrial departments; dedicated power supply from state utilities; building and occupancy approvals from local bodies; customs clearance for specialised equipment; chemical-storage approvals; and sector-specific clearances tied to incentive disbursement.²⁰ The interaction effects among these approval streams, particularly the misalignment between central environmental clearance and state industrial approvals, can extend project timelines materially. For a fab whose equipment ordering must align precisely with facility readiness on a foreign partner's construction schedule, such delays are not an inconvenience but a determinant of whether the project proceeds at all.

B. The inadequacy of the single window

The mission has been designated as a single window for incentive-related approvals, but it possesses convening power rather than decisional authority over line ministries. An investor must still separately engage the environmental ministry for clearances, state governments for land and power, and customs for equipment imports. The single window is therefore, in practice, a coordination desk rather than a genuine one-stop authority with time-bound service-delivery mandates backed by deemed-approval provisions. The comparative contrast is instructive: jurisdictions that have succeeded in attracting fabs have generally paired their incentives with permitting machinery capable of delivering clearances in months rather than years, a capacity that India's present arrangement does not reliably provide.

C. Customs and duty anomalies

Fabrication equipment, lithography, etch, deposition and planarisation systems, is among the most sophisticated manufactured goods in existence and is not available domestically. Where customs duty is levied on such equipment, and where the administrative process for claiming exemptions is cumbersome, the result is cash-flow pressure during the capital-intensive construction phase and distortion of the investment calculus, compounded by duty-inversion effects where components attract higher duties than finished goods. Predictable, zero-duty treatment of equipment that cannot be sourced domestically is a low-cost reform with a high signalling value to investors.

²⁰ Ministry of Env't, Forest & Climate Change, Environment Impact Assessment Notification, 2006, S.O. 1533(E), Govt. of India (2006), <https://environmentclearance.nic.in/writereaddata/EIA%20Notifications.pdf>.

These regulatory frictions share a defining feature: they are conjunctive rather than additive. A project that enjoys a generous incentive, secure land and reliable power is nonetheless unviable if its environmental clearance is unpredictable; one with rapid clearances and assured water cannot operate if customs delay starves it of process inputs; and none of these will attract a foreign licensor if intellectual-property protection is perceived as weak. Because the binding constraint is the weakest link rather than the average, the reliability of every input must be assured simultaneously, a property that distinguishes the regulation of semiconductor investment from ordinary industrial facilitation and that makes execution, rather than incentive design, the decisive variable.

VI. ENVIRONMENTAL AND WATER CHALLENGES

Semiconductor fabrication is among the most water- and chemical-intensive industrial processes in existence, and the environmental framework governing it must be simultaneously rigorous and predictable, a combination India's present system does not reliably deliver.

A. Water availability and ultra-pure water

The water demand of a fab is exceptional. A World Economic Forum analysis records that an average chip-manufacturing facility can use on the order of ten million gallons of ultra-pure water per day, comparable to the consumption of tens of thousands of households, and that producing ultra-pure water itself consumes substantially more municipal water than it yields.²¹ A United States International Trade Commission briefing notes that creating an integrated circuit on a single 300-millimetre wafer requires an estimated 2,200 gallons of water.²² Peer-reviewed survey data place the average water-use intensity of fabrication at 8.22 litres per square centimetre of processed wafer.²³ India's leading fab sites face divergent but equally serious water constraints: Dholera, in a semi-arid coastal zone, depends on managed allocation from a regional grid whose interruption would jeopardise operations, while water-rich Assam lacks the industrial-grade treatment and ultra-pure-water infrastructure that fabs require. The policy implication is that the state must pre-invest in source-water infrastructure, reservoirs, dedicated pipelines and tertiary treatment, rather than leaving each investor to build it from scratch, and must embody long-term raw-water allocations in enforceable commitments.

²¹ Kate James, *The Water Challenge for Semiconductor Manufacturing: What Needs to Be Done?*, World Econ. Forum (July 19, 2024), <https://www.weforum.org/stories/2024/07/the-water-challenge-for-semiconductor-manufacturing-and-big-tech-what-needs-to-be-done/>.

²² Lin Jones & Samantha Krulikowski, *Taiwan—The Silicon Island*, U.S. Int'l Trade Comm'n, Off. of Econ., Exec. Briefing on Trade (Feb. 2024), https://www.usitc.gov/publications/332/executive_briefings/ebot_silicon_island_taiwan_semiconductor.pdf.

²³ Yang Wu et al., *Environmental Data and Facts in the Semiconductor Manufacturing Industry: An Unexpected High Water and Energy Consumption Situation*, 4 Water Cycle 47, 47-54 (2023).

B. Calibrating environmental clearance

The Environment Impact Assessment Notification, 2006, issued under the *Environment (Protection) Act, 1986*, classifies projects and prescribes screening, scoping, public consultation and appraisal, procedures that for large industrial projects can take a considerable period.²⁴ That rigour is appropriate, but the environmental profile of a fab differs from that of, say, a mine or a thermal plant: its chemical footprint, properly managed, is contained, and a high proportion of its water can be recirculated. The appropriate response is not to exempt fabs from scrutiny but to create a dedicated, fast-tracked clearance category for semiconductor facilities, with pre-approved environmental-management frameworks, third-party auditing and continuous monitoring, an approach that preserves environmental rigour while delivering the predictability investors require. Predictability and protection are complementary objectives, not competing ones.

C. Chemical-waste management

Fabs generate distinctive waste streams, spent acid baths, photoresist solvents and developers, planarisation slurries and reject water, whose disposal in India must proceed through approved treatment, storage and disposal facilities. In the states hosting fab investment, the capacity and proximity of such facilities is a real constraint that should be addressed through pre-investment by state industrial-development corporations, so that waste-management infrastructure is in place before, not after, a plant becomes operational.

VII. LAND AND INFRASTRUCTURE

Land acquisition and infrastructure provisioning have historically been among the gravest obstacles to large-scale manufacturing in India, and the semiconductor sector's requirements, large, contiguous, vibration-controlled sites served by ultra-reliable utilities, exceed those of any other industrial category.

A. Land requirements and acquisition

A leading-edge fab occupies a substantial footprint together with associated utilities, storage and staff facilities, on a site that must be flat, vibration-controlled and of high load-bearing capacity. Greenfield sites meeting these specifications are scarce, and acquiring them through the framework of the Right to Fair Compensation and Transparency in Land Acquisition, Rehabilitation and Resettlement Act, 2013, which mandates social-impact assessment, consent

²⁴ Ministry of Env't, Forest & Climate Change, Environment Impact Assessment Notification, 2006, S.O. 1533(E), Govt. of India (2006), <https://environmentclearance.nic.in/writereaddata/EIA%20Notifications.pdf>.

thresholds and rehabilitation obligations, is necessarily deliberate.²⁵ The Dholera Special Investment Region offers a more efficient model in which the state acts as land aggregator and developer, pooling land and leasing developed plots to investors; the recent amendment of the Special Economic Zones rules to reduce the minimum land threshold for semiconductor zones from fifty to ten hectares points in the same pragmatic direction.²⁶ The principle that should be generalised is that land must be assembled and de-risked by the state before a project is offered, rather than left as a residual risk borne by the investor.

B. Power reliability and quality

Fabrication demands power of exceptional reliability and quality; a single unplanned interruption during a fabrication run can destroy an entire wafer batch of substantial value, and electricity constitutes the dominant share of a fab's energy use, with average energy intensity reported at 1.15 kilowatt-hours per square centimetre of wafer.²⁷ Meeting these requirements implicates dedicated high-voltage feeders, on-site backup generation, uninterruptible-power systems and long-term power-purchase arrangements, and, given the carbon intensity of fabrication and investors' decarbonisation commitments, access to firm renewable supply through open-access mechanisms. These are matters of electricity regulation and the performance of state distribution utilities, and thus squarely within the domain of regulatory execution.

C. Logistics and connectivity

Semiconductor supply chains depend on the just-in-time delivery of imported gases, chemicals and equipment, which in turn requires proximity to air-freight capacity and to compliant hazardous-goods handling and storage. India's designated fab sites are being developed with connectivity infrastructure, but last-mile logistics for hazardous materials remain underdeveloped, and dedicated chemical corridors and integrated logistics parks adjacent to fab sites are a necessary public investment.

VIII. INTELLECTUAL PROPERTY PROTECTION

Technology transfer is the fulcrum of semiconductor investment. When a foreign foundry licenses a process technology to an Indian partner, or an equipment vendor ships an advanced

²⁵ Right to Fair Compensation and Transparency in Land Acquisition, Rehabilitation and Resettlement Act, No. 30 of 2013, India Code (2013), <https://www.indiacode.nic.in/handle/123456789/2121>.

²⁶ Ministry of Commerce & Indus., *Government Notifies India's First Chip Fabrication Plant at SEZ Dholera*, Press Info. Bureau, Govt. of India (Apr. 16, 2026), <https://www.pib.gov.in/PressReleasePage.aspx?PRID=2252649>.

²⁷ Yang Wu et al., *Environmental Data and Facts in the Semiconductor Manufacturing Industry: An Unexpected High Water and Energy Consumption Situation*, 4 Water Cycle 47, 47-54 (2023).

lithography system, it entrusts its most valuable assets to the Indian legal system. If that system cannot reliably protect semiconductor intellectual property, through patents, layout-design rights, trade secrets and the enforcement of licensing terms, the transfer that the mission depends upon will not occur.

A. The current gap

India's intellectual-property framework has matured considerably, but gaps relevant to the semiconductor context remain. Section 3(k) of the *Patents Act, 1970* excludes a computer programme "per se" and algorithms from patentability, creating ambiguity around the firmware and embedded software integral to chip design.²⁸ The Semiconductor Integrated Circuits Layout-Design Act, 2000, enacted to give effect to India's obligations under the World Trade Organization's agreement on trade-related aspects of intellectual-property rights, has remained largely dormant, with no significant body of registration or enforcement practice developing in the quarter-century since its enactment.²⁹ Most consequentially, India has no standalone statute protecting trade secrets; protection rests on the law of contract and the common-law action for breach of confidence, an arrangement that offers uncertain deterrence against the misappropriation of process know-how.³⁰ Long patent-examination pendency further compounds the uncertainty that discourages technology-intensive investment.

B. Reforming the layout-design regime

An effective semiconductor intellectual-property ecosystem requires that the layout-design statute be operationalised in practice rather than merely enacted on paper. This entails a functioning registration system with online filing and expedited processing, a dedicated enforcement capability with sector-specific technical expertise, and civil and criminal remedies for the infringement of mask works commensurate with the very large design investment that a complex layout can represent. A right that exists in statute but not in administrable practice provides no assurance to a prospective licensor.

C. A trade-secrets framework

India would benefit from a standalone trade-secrets statute modelled on established international instruments, the United States' Defend Trade Secrets Act of 2016 and the European Union's Trade Secrets Directive of 2016, which together illustrate the now-conventional

²⁸ The Patents Act, 1970, No. 39 of 1970, § 3(k), India Code (1970), <https://www.indiacode.nic.in/bitstream/123456789/1392/1/A1970-39.pdf>.

²⁹ The Semiconductor Integrated Circuits Layout-Design Act, 2000, No. 37 of 2000, India Code (2000), <https://www.indiacode.nic.in/handle/123456789/1998>.

³⁰ AZB & Partners, *Trade Secrets: India* (2020), <https://www.azbpartners.com/bank/trade-secrets-india/>.

architecture of such protection.³¹ Key elements would include a statutory definition of a trade secret encompassing process recipes, equipment-configuration parameters and design databases; civil remedies including interlocutory injunctions and damages; criminal liability for intentional theft; and employee-mobility provisions calibrated to a knowledge-intensive sector. Such a statute would directly address the single greatest legal anxiety of a foreign licensor contemplating the transfer of fabrication know-how to India.

D. Governing technology-transfer agreements

Beyond the substantive law, the enforceability of the agreements through which technology is transferred is decisive. Licensors require confidence that choice-of-law and arbitration clauses will be respected, that international arbitral awards will be recognised and enforced, and that royalty and technical-service payments may be remitted without discretionary obstruction. A bilateral intellectual-property cooperation framework of the kind contemplated under the iCET, incorporating specific semiconductor-technology-protection undertakings, would reinforce these assurances at the inter-governmental level.³²

IX. TALENT DEVELOPMENT

India produces one of the world's largest pools of engineering graduates, yet the number with semiconductor-specific expertise, in very-large-scale-integration design, process engineering, device physics, equipment engineering, yield management and fab operations, is critically small relative to the tens of thousands of specialists the mission's targets would require. The gap is not generic but highly specific, and closing it is a project of seven to ten years that must begin immediately.

A. The nature of the shortfall

Fabs require engineers conversant with photolithography, plasma etch, vapour deposition, ion implantation and planarisation; assembly facilities require expertise in die-attach, wire-bonding and advanced packaging; design houses require register-transfer-level, analog and physical-design specialists and verification engineers. India's universities, for all their strength in software, have not historically produced these specialists at scale, and laboratory infrastructure

³¹ Defend Trade Secrets Act of 2016, Pub. L. No. 114-153, 130 Stat. 376 (2016), <https://www.govinfo.gov/content/pkg/PLAW-114publ153/html/PLAW-114publ153.htm>; Council Directive 2016/943, 2016 O.J. (L 157) 1 (EU), <https://eur-lex.europa.eu/eli/dir/2016/943/oj>.

³² The White House, *Fact Sheet: United States and India Elevate Strategic Partnership with the Initiative on Critical and Emerging Technology (iCET)* (Jan. 31, 2023), <https://bidenwhitehouse.archives.gov/briefing-room/statements-releases/2023/01/31/fact-sheet-united-states-and-india-elevate-strategic-partnership-with-the-initiative-on-critical-and-emerging-technology-icet/>.

for hands-on process-engineering training is largely absent. This is a deficit of specialised capacity, not of raw talent, and it is therefore remediable through deliberate institution-building.

B. A talent-development framework

A dedicated semiconductor talent programme should combine several instruments: centres of excellence in semiconductor education co-hosted at leading technical institutions and equipped with functioning process laboratories; faculty-development fellowships providing international training and industry placement; industry-sponsored academic chairs that keep curricula aligned with practice; mandatory apprenticeship pathways attached to incentive-approved projects to build a technician-grade workforce trained on-site; and a structured effort to mobilise the global diaspora of India-origin semiconductor professionals through enhanced residency benefits, research grants and leadership opportunities. These measures address the "contextual" dimension of capacity, the local absorptive capability without which even well-funded facilities underperform, that the comparative literature identifies as a frequent cause of ecosystem failure.³³

C. Design as the near-term advantage

India's comparative advantage in talent lies in chip design, where its software-engineering depth and mathematical training are most directly transferable. Design activity is capital-light relative to fabrication, generates high-value employment, and builds the domestic demand base that helps justify upstream investment. The Design Linked Incentive should accordingly be expanded and accelerated, treating design capability not as a consolation for the difficulty of fabrication but as a strategic asset in its own right.³⁴

X. CENTRE-STATE COORDINATION

India's constitutional architecture distributes the relevant competences across the Union and the States: industrial development is a concurrent subject, land is a State subject, and strategic national industries fall within Union jurisdiction. Semiconductor manufacturing sits at the intersection of all three and of multiple central ministries and state departments, and coordination failure across this matrix is the single most under-addressed challenge in India's semiconductor-policy discourse.

³³ Hui Hu et al., *Managing Technological Sovereignty: A Systematic Review of Semiconductor Industry Policy and Regional Ecosystem Governance*, 11 *Frontiers in Rsch. Metrics & Analytics*, art. 1762083 (2026).

³⁴ Ministry of Electronics & Info. Tech., *Government of India Taking Steps to Encourage Domestic Manufacturing of Semiconductors*, Press Info. Bureau, Govt. of India (July 31, 2024), <https://www.pib.gov.in/PressReleaseIframePage.aspx?PRID=2039638>.

A. The federalism problem

The reliance on high-level political intervention to conclude individual investments is not sustainable. When major projects have been secured, success has often required the personal involvement of the highest political offices at both the Union and State levels, a level of attention that cannot be replicated for every project in a growing pipeline. Institutional mechanisms must therefore be built to enable routine coordination at the administrative level without constant political escalation.

B. A standing coordination council

India should establish a permanent inter-governmental coordination council for the semiconductor sector, chaired at senior official level within the lead ministry and including the finance, commerce and external-affairs ministries, the environmental ministry, nodal officers from semiconductor-hosting States, and representatives of approved projects. Such a body, meeting on a regular cycle with a mandate to resolve escalated project-specific issues within a defined period, would convert episodic political problem-solving into a predictable administrative process.

C. Harmonising State incentives

Multiple States have announced semiconductor-specific incentive policies. This competition is healthy in principle but can generate regulatory ambiguity where central and state incentives overlap, or disappointment where States under-deliver on infrastructure commitments made to attract projects. The Union should publish a model State semiconductor-policy template ensuring consistency on land-provision terms, power-tariff treatment, water-allocation commitments, state-level clearance timelines and stamp-duty treatment, which States could adopt as a condition of project routing.

D. Accountability mechanisms

Most importantly, incentive disbursement should be conditioned on State performance against defined metrics, land handed over, power commissioned, water operationalised and state-level clearances granted within agreed deadlines. States that miss these milestones should face consequences in incentive eligibility, while those that outperform should receive preference in the routing of future projects. This performance conditionality is the mechanism that converts incentive competition among the States into accountable partnership, and it directly addresses

the "governance failure" of misaligned incentives that the literature identifies as a principal cause of ecosystem disappointment.³⁵

XI. THE ROLE OF CORPORATE AFFAIRS AND GOVERNMENT RELATIONS

The sector's interface with the Indian regulatory state extends well beyond industrial policy into foreign-investment regulation, competition policy and the practice of government relations, and the quality of a firm's navigation of these domains contributes materially to project success.

A. Foreign-investment and exchange regulation

Semiconductor investment from foreign firms flows under India's foreign-investment regime, but technology-transfer agreements with particular royalty and repatriation structures can attract scrutiny under exchange-management and external-borrowing rules. Sector-specific guidance clarifying permissible royalty structures for semiconductor licences, acceptable terms for technical-services agreements, and approval-free thresholds for sector-specific payments would reduce a recurring source of friction and reinforce the assurances that licensors require, complementing the intellectual-property reforms discussed above.

B. Competition-policy considerations

The global consolidation of the industry, concentrated foundry capacity, a near-monopoly in the most advanced lithography, and a handful of dominant equipment and materials suppliers, raises competition-policy questions as Indian firms build their positions. The competition authority would benefit from sector-specific analytical capacity addressing merger assessment in semiconductor supply chains, exclusivity provisions in technology licences, and the treatment of standard-essential patents, so that complex and technically demanding cases can be adjudicated with the requisite expertise.

C. Government-relations strategy

Firms participating in the ecosystem must invest in government-relations capabilities that go well beyond conventional advocacy. Effective engagement requires the capacity to brief officials and ministers on semiconductor processes and investment requirements in accessible terms; the management of relationships simultaneously across multiple central ministries, the relevant offices and State governments; systematic monitoring of draft regulations and notifications affecting fab operations; and coalition-building through industry bodies to present unified positions. Where the binding constraints on the sector are regulatory, these functions are

³⁵ Hui Hu et al., *Managing Technological Sovereignty: A Systematic Review of Semiconductor Industry Policy and Regional Ecosystem Governance*, 11 *Frontiers in Rsch. Metrics & Analytics*, art. 1762083 (2026).

strategic rather than merely administrative, and they operate as a private complement to public governance, surfacing implementation gaps early and constructively. Recognising corporate-affairs and government-relations capacity as part of national ecosystem infrastructure, rather than as overhead, is itself part of the institutional maturation the sector requires.

XII. POLICY RECOMMENDATIONS

The following recommendations are organised by horizon and are intended to be operationally specific rather than aspirational, on the premise that India's deficit is more often one of implementation than of conception. They are offered as reasoned proposals consistent with the verified evidence.

In the immediate term, the mission should be empowered with time-bound, deemed-approval authority over central clearances for approved projects, with automatic escalation on default; the layout-design statute should be operationalised through a functioning registration office and digital portal; a dedicated, fast-tracked environmental-clearance category for semiconductor facilities should be created by notification, with pre-approved management frameworks and third-party monitoring; and equipment that cannot be sourced domestically should receive predictable zero-duty treatment.³⁶ In parallel, a national semiconductor talent programme should be launched, with centres of excellence at leading technical institutions and expedited residency pathways for diaspora professionals.

Over the medium term, the State should commission ultra-pure-water and chemical-waste infrastructure at designated industrial parks ahead of investor entry; negotiate long-term power-purchase arrangements with guaranteed-uptime obligations; extend the land-pooling model of the Dholera region to other sites; introduce a standalone trade-secrets statute drawing on established international models; deepen bilateral intellectual-property cooperation under the iCET framework; reduce patent-examination pendency through additional examiner capacity and modern search tools; and establish the standing Centre-State coordination council with performance-conditioned incentive disbursement.³⁷

³⁶ The Semiconductor Integrated Circuits Layout-Design Act, 2000, No. 37 of 2000, India Code (2000), <https://www.indiacode.nic.in/handle/123456789/1998>; Ministry of Env't, Forest & Climate Change, Environment Impact Assessment Notification, 2006, S.O. 1533(E), Govt. of India (2006), <https://environmentclearance.nic.in/writereaddata/EIA%20Notifications.pdf>.

³⁷ Kate James, *The Water Challenge for Semiconductor Manufacturing: What Needs to Be Done?*, World Econ. Forum (July 19, 2024), <https://www.weforum.org/stories/2024/07/the-water-challenge-for-semiconductor-manufacturing-and-big-tech-what-needs-to-be-done/>; Defend Trade Secrets Act of 2016, Pub. L. No. 114-153, 130 Stat. 376 (2016), <https://www.govinfo.gov/content/pkg/PLAW-114publ153/html/PLAW-114publ153.htm>; Council Directive 2016/943, 2016 O.J. (L 157) 1 (EU), <https://eur-lex.europa.eu/eli/dir/2016/943/oj>; The White House, *Fact Sheet: United States and India Elevate Strategic Partnership with the Initiative on Critical and Emerging Technology (iCET)* (Jan. 31, 2023), <https://bidenwhitehouse.archives.gov/briefing-room/statements-releases/2023/01/31/fact-sheet-united-states-and-india-elevate-strategic-partnership-with-the-initiative-on-critical-and-emerging-technology/>

As a structural matter over the longer term, India should invest in a public-private semiconductor research consortium of the kind exemplified internationally by IMEC in Belgium and, historically, by SEMATECH in the United States, focused on process development with shared intellectual property; create a specialised long-term project-finance window to reduce dependence on higher-cost commercial lending; develop a semiconductor-focused free-trade-zone regime with expedited customs and bonded warehousing for chemicals and gases; and establish a calibrated national export-control system aligned with multilateral arrangements, so as to qualify for broader technology-transfer reciprocity with allied jurisdictions.³⁸

XIII. CONCLUSION

India's semiconductor ambition is not a fantasy. The geopolitical tailwinds are real, the incentive architecture is in place, and the first projects are operational. But the gap between ambition and execution has historically been the graveyard of Indian industrial-policy visions, and the difference this time must be institutional. India needs not merely better policies but better policy-delivery mechanisms: time-bound clearances with legal consequences for delay, performance-conditioned intergovernmental transfers, intellectual-property frameworks that foreign technology holders can trust, talent pipelines that produce semiconductor engineers at scale, and infrastructure investments that arrive before the fab rather than years after it.³⁹

The comparative record reinforces the point. Subsidy has become a universal instrument, matched across every serious jurisdiction, and is therefore no longer a source of durable advantage; what distinguishes successful ecosystems is the reliability of their execution and the depth of their institutions, from Taiwan's accreted research and supplier base to the coordinated cluster planning of its East-Asian peers.⁴⁰ India's window is real but finite, and missing it would not merely delay its ambitions but allow competing jurisdictions to consolidate supply chains

emerging-technology-icet/.

³⁸ imec, *About imec*, <https://www.imec-int.com/en/about-us> (last visited June 2026); Def. Advanced Rsch. Projects Agency, *SEMATECH (Innovation Timeline)*, <https://www.darpa.mil/about/innovation-timeline/sematech> (last visited June 2026); The White House, *Fact Sheet: 2024 Quad Leaders' Summit* (Sept. 21, 2024), <https://bidenwhitehouse.archives.gov/briefing-room/statements-releases/2024/09/21/fact-sheet-2024-quad-leaders-summit/>.

³⁹ Chad P. Bown & Dan Wang, *Semiconductors and Modern Industrial Policy*, 38 J. Econ. Persp. 81, 81-110 (2024); Org. for Econ. Co-operation & Dev., *Recent Trends in Semiconductor Subsidies* (OECD Policy Briefs 2025), <https://doi.org/10.1787/5e91af33-en>.

⁴⁰ Org. for Econ. Co-operation & Dev., *Recent Trends in Semiconductor Subsidies* (OECD Policy Briefs 2025), <https://doi.org/10.1787/5e91af33-en>; Lin Jones & Samantha Krulikowski, *Taiwan—The Silicon Island*, U.S. Int'l Trade Comm'n, Off. of Econ., Exec. Briefing on Trade (Feb. 2024), https://www.usitc.gov/publications/332/executive_briefings/ebot_silicon_island_taiwan_semiconductor.pdf; William A. Reinsch & Jack Whitney, *Silicon Island: Assessing Taiwan's Importance to U.S. Economic Growth and Security*, Ctr. for Strategic & Int'l Studies (Jan. 10, 2025), <https://www.csis.org/analysis/silicon-island-assessing-taiwans-importance-us-economic-growth-and-security>.

around their own anchors. The architecture proposed here is implementable; the open question is whether India's institutions, its bureaucracies, courts, universities and State governments, can marshal the coordinated urgency that the transition from a software-services economy to a hardware-capable one requires. If they can, the journey from silicon to sovereignty will be completed not by the eloquence of policy documents but by the clearances that are honoured, the water plants that are built before the fab opens, the trade-secret cases that produce a credible deterrent, and the engineers who emerge equipped to run a modern foundry, and the Semiconductor Mission can become a durable platform for responsible innovation, regulatory excellence and long-term growth.

XIV. BIBLIOGRAPHY

1. Arcuri, G., & Lu, S. (2022, March 22). Taiwan's semiconductor dominance: Implications for cross-strait relations and the prospect of forceful unification. Center for Strategic and International Studies. <https://www.csis.org/blogs/perspectives-innovation/taiwans-semiconductor-dominance-implications-cross-strait-relations>
2. AZB & Partners. (2020). Trade secrets: India. <https://www.azbpartners.com/bank/trade-secrets-india/>
3. Bown, C. P., & Wang, D. (2024). Semiconductors and modern industrial policy. *Journal of Economic Perspectives*, 38(4), 81-110. <https://doi.org/10.1257/jep.38.4.81>
4. Bureau of Industry and Security. (2022, October 13). Implementation of additional export controls: Certain advanced computing and semiconductor manufacturing items; supercomputer and semiconductor end use; entity list modification. *Federal Register*, 87(197). <https://www.federalregister.gov/documents/2022/10/13/2022-21658/implementation-of-additional-export-controls-certain-advanced-computing-and-semiconductor>
5. Burkacky, O., Dragon, J., & Lehmann, N. (2022, April 1). The semiconductor decade: A trillion-dollar industry. McKinsey & Company. <https://www.mckinsey.com/industries/semiconductors/our-insights/the-semiconductor-decade-a-trillion-dollar-industry>
6. CHIPS and Science Act of 2022, Pub. L. No. 117-167, 136 Stat. 1366 (2022). <https://www.govinfo.gov/content/pkg/PLAW-117publ167/html/PLAW-117publ167.htm>

7. Defend Trade Secrets Act of 2016, Pub. L. No. 114-153, 130 Stat. 376 (2016). <https://www.govinfo.gov/content/pkg/PLAW-114publ153/html/PLAW-114publ153.htm>
8. Defense Advanced Research Projects Agency. (n.d.). SEMATECH (Innovation timeline). Retrieved June 2026, from <https://www.darpa.mil/about/innovation-timeline/sematech>
9. Directive (EU) 2016/943 of the European Parliament and of the Council of 8 June 2016 on the protection of undisclosed know-how and business information (trade secrets) against their unlawful acquisition, use and disclosure. (2016). Official Journal of the European Union, L 157, 1-18. <https://eur-lex.europa.eu/eli/dir/2016/943/oj>
10. European Union. (2024). Strengthening the EU's semiconductor ecosystem – Chips Act [Summary of legislation]. EUR-Lex, Publications Office of the European Union. <https://eur-lex.europa.eu/EN/legal-content/summary/strengthening-the-eu-s-semiconductor-ecosystem-chips-act.html>
11. Goldberg, P. K., Juhász, R., Lane, N. J., Lo Forte, G., & Thurk, J. (2024). Industrial policy in the global semiconductor sector (NBER Working Paper No. 32651). National Bureau of Economic Research. <https://doi.org/10.3386/w32651>
12. Hu, H., et al. (2026). Managing technological sovereignty: A systematic review of semiconductor industry policy and regional ecosystem governance. *Frontiers in Research Metrics and Analytics*, 11, Article 1762083. <https://doi.org/10.3389/frma.2026.1762083>
13. imec. (n.d.). About imec. Retrieved June 2026, from <https://www.imec-int.com/en/about-us>
14. India Semiconductor Mission. (n.d.). About SemiconIndia programme. Ministry of Electronics and Information Technology, Government of India. Retrieved June 2026, from <https://ism.gov.in/about-semiconindia>
15. James, K. (2024, July 19). The water challenge for semiconductor manufacturing: What needs to be done? World Economic Forum. <https://www.weforum.org/stories/2024/07/the-water-challenge-for-semiconductor-manufacturing-and-big-tech-what-needs-to-be-done/>
16. Jones, L., & Krulikowski, S. (2024, February). Taiwan—The silicon island (Executive Briefing on Trade). U.S. International Trade Commission, Office of Economics. https://www.usitc.gov/publications/332/executive_briefings/ebot_silicon_island_taiwan_semiconductor.pdf

17. Ministry of Commerce and Industry. (2026, April 16). Government notifies India's first chip fabrication plant at SEZ Dholera [Press release]. Press Information Bureau, Government of India. <https://www.pib.gov.in/PressReleasePage.aspx?PRID=2252649>
18. Ministry of Electronics and Information Technology. (2023, December 6). Micron's semiconductor project at Sanand in Gujarat on fast track [Press release]. Press Information Bureau, Government of India. <https://www.pib.gov.in/PressReleaseIframePage.aspx?PRID=1983128>
19. Ministry of Electronics and Information Technology. (2024, July 31). Government of India taking steps to encourage domestic manufacturing of semiconductors [Press release]. Press Information Bureau, Government of India. <https://www.pib.gov.in/PressReleaseIframePage.aspx?PRID=2039638>
20. Ministry of Electronics and Information Technology. (2024, September 2). Cabinet approves one more semiconductor unit under India Semiconductor Mission (ISM) [Press release]. Press Information Bureau, Government of India. <https://www.pib.gov.in/PressReleaseIframePage.aspx?PRID=2050859>
21. Ministry of Electronics and Information Technology. (2026, May 5). Cabinet approves two more semiconductor manufacturing units [Press release]. Press Information Bureau, Government of India. <https://www.pib.gov.in/PressReleasePage.aspx?PRID=2258119>
22. Ministry of Environment, Forest and Climate Change. (2006). Environment Impact Assessment Notification, 2006 (S.O. 1533(E)). Government of India. <https://environmentclearance.nic.in/writereaddata/EIA%20Notifications.pdf>
23. Ministry of External Affairs (Economic Diplomacy Division). (2025, February 12). India's semiconductor market set to reach \$103.4 billion by 2030. IndBiz, Government of India. <https://indbiz.gov.in/indias-semiconductor-market-set-to-reach-103-4-billion-by-2030/>
24. Organisation for Economic Co-operation and Development. (2025). Recent trends in semiconductor subsidies (OECD Policy Briefs). OECD Publishing. <https://doi.org/10.1787/5e91af33-en>
25. Prime Minister's Office. (2026, February 28). Prime Minister inaugurates Micron Technology's semiconductor ATMP facility in Sanand, Gujarat [Press release]. Press Information Bureau, Government of India. <https://www.pib.gov.in/PressReleasePage.aspx?PRID=2233998>

26. Reinsch, W. A., & Whitney, J. (2025, January 10). Silicon island: Assessing Taiwan's importance to U.S. economic growth and security. Center for Strategic and International Studies. <https://www.csis.org/analysis/silicon-island-assessing-taiwans-importance-us-economic-growth-and-security>
27. Right to Fair Compensation and Transparency in Land Acquisition, Rehabilitation and Resettlement Act, No. 30 of 2013, India Code (2013). <https://www.indiacode.nic.in/handle/123456789/2121>
28. Semiconductor Industry Association, & Boston Consulting Group. (2021). Strengthening the global semiconductor supply chain in an uncertain era. <https://www.semiconductors.org/strengthening-the-global-semiconductor-supply-chain-in-an-uncertain-era/>
29. Semiconductor Industry Association. (2023). 2023 state of the U.S. semiconductor industry. https://www.semiconductors.org/wp-content/uploads/2023/08/SIA_State-of-Industry-Report_2023_Final_080323.pdf
30. Shivakumar, S., Wessner, C., & Howell, T. (2026, March 24). China's localization drive in semiconductors gains impetus from allied chip export controls. Center for Strategic and International Studies. <https://www.csis.org/analysis/chinas-localization-drive-semiconductors-gains-impetus-allied-chip-export-controls>
31. The Patents Act, 1970, No. 39 of 1970, § 3(k), India Code (1970). <https://www.indiacode.nic.in/bitstream/123456789/1392/1/A1970-39.pdf>
32. The Semiconductor Integrated Circuits Layout-Design Act, 2000, No. 37 of 2000, India Code (2000). <https://www.indiacode.nic.in/handle/123456789/1998>
33. The White House. (2023, January 31). Fact sheet: United States and India elevate strategic partnership with the initiative on Critical and Emerging Technology (iCET). <https://bidenwhitehouse.archives.gov/briefing-room/statements-releases/2023/01/31/fact-sheet-united-states-and-india-elevate-strategic-partnership-with-the-initiative-on-critical-and-emerging-technology-icet/>
34. The White House. (2024, September 21). Fact sheet: 2024 Quad Leaders' Summit. <https://bidenwhitehouse.archives.gov/briefing-room/statements-releases/2024/09/21/fact-sheet-2024-quad-leaders-summit/>
35. U.S. National Institute of Standards and Technology. (2024). CHIPS for America fact sheet: Federal programs supporting the U.S. semiconductor supply chain and workforce.

- U.S. Department of Commerce. <https://www.nist.gov/document/chips-america-fact-sheet-federal-incentives>
36. Union Cabinet. (2024, February 29). Giant leap for India Semiconductor Mission: Cabinet approves three more semiconductor units [Press release]. Press Information Bureau, Government of India. <https://www.pib.gov.in/PressReleasePage.aspx?PRID=2010132>
37. Wu, Y., et al. (2023). Environmental data and facts in the semiconductor manufacturing industry: An unexpected high water and energy consumption situation. *Water Cycle*, 4(1), 47-54. <https://doi.org/10.1016/j.watcyc.2023.01.004>
